

# TRANSMITTAL FORM

(To be used for all correspondence after initial filing)

<b>TRANSMITTAL FORM</b> (To be used for all correspondence after initial filing)		Application Number	10/645,932
		Filing Date	August 20, 2003
		First Named Inventor	Luo, Mei
		Art Unit	To Be Assigned
		Examiner Name	To Be Assigned
Total Number of Pages in This Submission	7	Attorney Docket Number	015114-067900US

## ENCLOSURES (Check all that apply)

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## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	Townsend and Townsend and Crew LLP Steven Cahill	Reg. No. 44,578
Signature		
Date	March 10, 2004	

## CERTIFICATE OF TRANSMISSION/MAILING

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TOWNSEND and TOWNSEND and CREW LLP

By: Edward Marmar



PATENT  
Attorney Docket No.: 015114-067900US  
Client Reference No.: A1073

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Mei Luo et al.

Application No.: 10/645,932

Filed: August 20, 2003

For: DYNAMICALLY ADJUSTABLE  
TERMINATION IMPEDANCE  
CONTROL TECHNIQUES

Examiner: To Be Assigned

Art Unit: To Be Assigned

SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT UNDER 37  
CFR §1.97 and §1.98

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P.O. Box 1450  
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Sir:

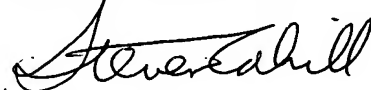
The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of Reference Nos. 55-63 are enclosed herewith. Reference Nos. 1-54 are not enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement.

However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



Steven Cahill  
Reg. No. 44,578

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60161656 v1

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet

1

of

3

**Complete if Known**

Application Number	10/645,932
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Examiner Name	To Be Assigned
Attorney Docket Number	015114-067900US

**U.S. PATENT DOCUMENTS+**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	0001	US-4,719,369	01-12-1988	Asano et al.	
	0002	US-4,954,729	09-04-1990	Urai	
	0003	US-5,111,081	05-05-1992	Atallah	
	0004	US-5,134,311	07-28-1992	Biber et al.	
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	0007	US-5,359,235	10-25-1994	Coyle et al.	
	0008	US-5,374,861	12-20-1994	Kubista	
	0009	US-5,592,510	01-07-1997	Van Brunt et al.	
	0010	US-5,602,494	02-11-1997	Sundstrom	
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	0015	US-5,864,715	01-26-1999	Zani et al.	
	0016	US-5,939,896	08-17-1999	Hedberg	
	0017	US-5,955,911	09-21-1999	Drost et al.	
	0018	US-5,970,255	10-19-1999	Tran et al.	
	0019	US-6,008,665	12-28-1999	Kalb et al.	
	0020	US-6,026,456	02-15-2000	Ilkbahar	
	0021	US-6,037,798	03-14-2000	Hedberg	
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	0025	US-6,097,208	08-01-2000	Okajima et al.	
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	0029	US-6,154,060	11-28-2000	Morriss	
	0030	US-6,157,206	12-05-2000	Taylor et al.	
	0031	US-6,181,157 B1	01-30-2001	Fiedler	
	0032	US-6,236,231 B1	05-22-2001	Nguyen	
	0033	US-6,252,419 B1	06-26-2001	Sung et al.	

Examiner  
SignatureDate  
Considered

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60161656 v1

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			Application Number	10/645,932	
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Sheet	2	of	3	Attorney Docket Number	015114-067900US

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Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code <sup>2</sup> (if known)			
	0034	US-6,329,836 B1	12-11-2001	Drost et al.	
	0035	US-6,356,106 B1	03-12-2002	Greeff et al.	
	0036	US-6,362,644 B1	03-26-2002	Jeffrey et al.	
	0037	US-6,366,128 B1	04-02-2002	Ghia et al.	
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	0039	US-6,414,512 B1	07-02-2002	Moyer	
	0040	US-6,424,169 B1	07-23-2002	Partow et al.	
	0041	US-6,433,579 B1	08-13-2002	Wang et al.	
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	0043	US-6,448,813 B2	09-10-2002	Garlepp et al.	
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	0045	US-6,586,964 B1	07-01-2003	Kent et al.	
	0046	US-6,590,413 B1	07-08-2003	Yang	
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	0049	US-6,642,741 B2	11-04-2003	Metz et al.	
	0050	US 2002/0010853 A1	01-24-2002	Trimberger et al.	
	0051	US 2002/0060602 A1	05-23-2002	Ghia et al.	
	0052	US 2002/0101278 A1	08-01-2002	Schultz et al.	
	0053	US 2003/0062922 A1	04-03-2003	Douglass et al.	
	0054	US 2004/0008054 A1	01-15-2004	Lesea et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
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		Application Number	10/645,932		
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		First Named Inventor	Luo, Mei		
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Sheet	3	of	3	Attorney Docket Number	015114-067900US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	0055	Altera, Apex 20K "Programmable Logic Device Family," Altera Corporation, Ver. 1.1, May 2001	
	0056	Altera, Apex II "Programmable Logic Device Family," Altera Corporation, Ver. 1.1, May 2001	
	0057	Bendak, M. et al. (1996). "CMOS VLSI Implementation of Gigabyte/second computer network links," Dept. of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407, IEEE International Symposium on Circuits and Systems pp.269-272.	
	0058	Boni, A. et al. (2001). "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-um CMOS," IEEE Journal of Solid-State Circuits, 36(4):706-711.	
	0059	Esch and Manley, Theory and Design of CMOS HSTL I/O Pads, The Hewlett Packard Journal, Aug, 1998	
	0060	Xilinx, "Spartan-3 1.2V FPGA Family: Functional Description," Xilinx, DS099-2 (v1.2) July 11, 2003	
	0061	Xilinx, "Virtex-II 1.5V Field Programmable Gate Arrays," Xilinx, DSO3102 (v1.5), Apr. 2, 2001	
	0062	Xilinx, "Virtex-II Platform FPGAs: Detailed Description," Xilinx, DS031-2 (v3.1) October 14, 2003	
	0063	Xilinx, "Virtex-II Pro Platform FPGAs: Functional Description," Xilinx, DS083-2 (v2.9) October 14, 2003	

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